REMARKS

Claims 1-16 remain pending in the application.

Applicant acknowledges the indication that claims 4, 6, 10, 12, 14 and 16 define allowable subject matter and would be allowed if rewritten in independent form to include all limitations of their respective base claims, and any intervening claims.

Reexamination and reconsideration of the application are respectfully requested in view of the following Remarks.

35 U.S.C. § 102

The Office Action rejects claims 1-3, 5, 7-9, 11, 13 and 15 under 35 U.S.C. § 102 over Toda U.S. Patent 6,363,465 ("Toda").

Applicant respectfully traverses these rejections for at least the following reasons.

Claim 1

The data pipeline circuit of claim 1 includes: (1) a control signal generating unit adapted to receive a clock signal and adapted to output a control signal, a first switching signal, and a second switching signal, according to a frequency of the clock signal; (2) a first transmitting unit adapted to receive data stored in a memory cell and to transmit data to an input/output driver in response to activation of the first switching signal and the second switching signal; and (3) a second transmitting unit adapted to transmit data to the input/output driver in response to activation of the control signal, wherein the first transmitting unit and the second transmitting unit are adapted to be alternatively activated.

Applicant respectfully submits that Toda does not disclose a data pipeline circuit as recited in claim 1 including such a combination of features.

The Office Action cites FIG. 2 of Toda, and states that:

- CK1 corresponds to the first switching signal
- CK2 corresponds to the second switching signal
- CK3 corresponds to the control signal

- Element 18 corresponds to the first transmitting unit
- Element 21 corresponds to the second transmitting unit
- Element 22 corresponds to the output driver.

Now, according to claim 1, the second transmitting unit is adapted to transmit data to the input/output driver in response to activation of the control signal.

However, in contrast, in Toda the element 21 (supposedly corresponding to the second transmitting unit) does not even receive the CK3 signal (supposedly corresponding to the control signal), and therefore cannot possibly be adapted ***to transmit data*** to element 22 (supposedly corresponding to the input/output driver) in response to activation of the CK3 signal (supposedly corresponding to the control signal).

So FIG. 2 of Toda cannot disclose the data pipeline circuit of claim 1.

Also, according to claim 1, the first transmitting unit is adapted to transmit data to an input/output driver in response to activation of the first switching signal and the second switching signal.

However, in contrast, in Toda element 18 (supposedly the first transmitting unit) does not even receive the CK2 signal (supposedly corresponding to the second switching signal) and therefore cannot possibly be adapted ***to transmit data*** element 22 (supposedly the input/output driver) in response to activation of the first switching signal and the second switching signal.

So, again, FIG. 2 of Toda cannot disclose the data pipeline circuit of claim 1.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 1 is clearly patentable over Toda.

Claims 2-3 and 5

Claims 2-3 and 5 depend from claim 1 and are deemed patentable over Toda for at least the reasons set forth above with respect to claim 1, and for the following additional reasons.

Claim 2

In the data pipeline circuit of claim 2, the first transmitting unit comprises: (1) a first switching circuit adapted to output data in response to activation of the first switching signal; (2) a latching circuit adapted to latch and output the output of the first switching circuit; and (3) a second switching circuit adapted to output the output of the latching circuit to the input/output driver in response to activation of the second switching signal.

Applicant respectfully submits that Toda does not disclose a data pipeline circuit as recited in claim 1 including such a combination of features.

The Office Action cites FIG. 2 of Toda, and states that:

- Element 18 corresponds to the first transmitting unit
- Element 18 corresponds to the first switching circuit
- Element 18 corresponds to the latching circuit
- Elements 21, 26 and 22 correspond to the second switching circuit

Now, according to claim 2, the first transmitting unit ***includes*** the second switching unit.

However, in contrast, in Toda the element 18 (supposedly corresponding to the first transmitting unit) very clearly and plainly ***does not include*** elements 21, 26 or 22 (supposedly corresponding to the second switching circuit.

So FIG. 2 of Toda cannot disclose data pipeline circuit of claim 2.

Also, according to the Office Action, element 18 supposedly corresponds to both the first switching circuit and the latching circuit. However, accordingly to claim 1, ***the latching circuit is adapted to latch and output the output of the first switching circuit***. Toda does not disclose or suggest, nor does it make any sense, that element 18 of Toda should "latch and output the output of" element 18!

So, again, FIG. 2 of Toda cannot disclose data pipeline circuit of claim 2.

Accordingly, for at least these additional reasons, Applicant respectfully

submits that claim 2 is clearly patentable over Toda.

Claim 7

Among other things, the device of claim 7 includes an input/output driver.

The Examiner cites element 22 of Toda.

Clearly, element 22 of Toda is only an output driver, not an input/output driver. It drives output signals. It does not drive any input signals.

So element 22 of Toda cannot possibly correspond to the recited input/output driver.

The Examiner is not free to interpret the term "input/output drive" any old way that he chooses. There are very specific rules providing the bases by which an Examiner is supposed to interpret the language in an Applicant's claim. None of those rules permit the Examiner to interpret something as being "analogous" to a something completely different. Indeed, it appears that the Examiner has totally ignored the well-established rules for proper interpretation of claim language.

No proper interpretation of the recited "input/output driver" can possibly read on element 22 of Toda.

Furthermore, in the device of claim 7 the input/output driver is adapted to receive first data from outside of the semiconductor memory device, in synchronization with a first clock signal, and adapted to output second data stored in the memory cell core, in synchronization with a second clock signal.

In contrast, it is extremely clear that output driver 22 does not receive any "first data from outside of the semiconductor memory device." In that regard, very clearly output driver 22 does not receive the control signal SLTC from outside of the semiconductor memory device, as mentioned in the Office Action, but instead the control signal SLTC (which is also not "first data") is "received" by controller 23 and not even provided at all to output driver 22.

So, again, element 22 of Toda cannot possibly correspond to the input/output driver of claim 7.

Therefore FIG. 2 of Toda cannot disclose the device of claim 1.

Furthermore, the device of claim 7 includes a control signal generating unit which is adapted to receive a first clock signal and a second clock signal, and which is adapted to output a control signal corresponding to frequencies of the first clock signal and the second clock signal.

The Office Action cites controller 23 of Toda as supposedly corresponding to the recited control signal generating unit.

Applicant respectfully disagrees.

As noted above, the control signal generating unit of claim 7 is adapted to receive a first clock signal and a second clock signal. In contrast, it is very clear from inspection of FIG. 2 that the controller 23 of Toda receives only one clock signal, CLK. The only other signal received by the controller 23 of Toda is the control signal SLTC which is not a clock signal, and is used to select a latency for the device. Absolutely nothing in the cited text at col. 2, lines 45-55 even remotely suggests that controller 23 receives both a first clock signal and a second clock signal.

Therefore, again, FIG. 2 of Toda cannot disclose the device of claim 1.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 7 is patentable over Toda.

Claims 8-9 and 11-13

Claims 8-9 and 11-13 depend from claim 7 and are deemed patentable over Toda for at least the reasons set forth above with respect to claim 7, and for the following additional reasons.

Claim 8

Among other things, in the device of claim 8, the control signal generating unit is adapted to detect a phase difference between the first clock signal and the second clock signal, and is adapted to output the control signal with a logic state based on a detected result.

Toda does not even remotely suggest such features.

The Office Action cites col. 26, lines 36-54.

However, the cited text does not disclose a control signal generating unit that is

adapted to detect a phase difference between a received first clock signal and a received second clock signal. Indeed, the cited text does not even disclose that a control signal generating unit is adapted to receive a first clock signal and a second clock signal! Instead, the cited text merely describes receiving one, singular, ("external") clock signal and generating therefrom a plurality of first clock signals in phase with the received clock signal, and a plurality of second clock signals delayed in phase with respect to the external clock signal. Of course this is not what s recited in claim 8.

Accordingly, for at least these additional reasons, Applicant respectfully submits that claim 8 is patentable over Toda.

Claim 9

Claim 9 recites similar features to those recited in claim 2 as discussed above. For the same reasons as those set forth above with respect to claim 2, Applicant respectfully submits that Toda does not disclose such a combination of features.

Accordingly, for at least these additional reasons, Applicant respectfully submits that claim 9 is patentable over Toda.

Claim 15

Among other things, the device of claim 15 includes an input/output driver.

Again, the Examiner cites element 22 of Toda.

Again, Applicant respectfully submits that output driver 22 of Toda is not an ***input***/output driver.

Therefore FIG. 2 of Toda cannot disclose the device of claim 15.

Also among other things, the device of claim 15 includes a control signal generating unit adapted to receive a first clock signal, a second clock signal, and information about operation modes of the semiconductor memory device, and which is adapted to output a first switching signal, a second switching signal, and a control signal corresponding to the first clock signal, the second clock signal, and information about the operation modes of the semiconductor memory device.

Again the Examiner cites element 23 of Toda.

Again Applicant respectfully submits that controller 23 of Toda does

As explained above with respect to claim 7, controller 23 of Toda receives only one clock signal, CLK, and nothing in the cited text at col. 2, lines 45-55 even remotely suggests that controller 23 receives both a first clock signal and a second clock signal.

Therefore, again, FIG. 2 of Toda cannot disclose the device of claim 15.

Finally, the device of claim 15 also includes an input/output data pipeline circuit that further includes a first transmitting unit, which is adapted to be activated in response to activation of the first switching signal and the second switching signal, and a second transmitting unit which is adapted to be activated in response to activation of the control signal.

As explained above with respect to claim 1, Toda does not disclose such a combination of features.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 15 is clearly patentable over Toda.

Claim 16

Claim 16 depends from claim 15 and is deemed patentable over Toda for at least the reasons set forth above with respect to claim 15, and also for similar reasons to those set forth above with respect to claim 8.

CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 1-16, and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283-0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No.

50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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